IN THE CLAIMS

1. (Presently amended): A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of ~~N signal~~ *N* clock phases;

- a data sampling component sampling a portion of said data signal causing a logic output statement based on a truth table, said data sampling component comprising

- a buffer component for buffering said data signal, said buffer component triggered by a first clock phase *i*, a second clock phase *j* and a third clock phase *k*, resulting in a buffering of the state of said data signal at said clock phases *i*, *j*, and *k* and wherein the clock phases *i*, *j*, and *k* are interdependent by at least one of the equations:

$$j = i + N/2 - M \text{ and } k = i + N/2 \text{ if } i \leq N/2 \text{ and}$$

$$j = i - N/2 - M \text{ and } k = i - N/2 + M \text{ if } \cancel{i}\ i > N/2$$

with a parameter *M* selectable within $0 < M < N/2$, and ~~comprising~~

- a phase detector ~~assigned~~ coupled to said buffer component; ~~,~~ and

~~a counter assigned to said phase detector with said logic output statement causing a reaction of said counter; and~~

- a phase selector ~~assigned to said counter~~ coupled to said data sampling component~~, wherein~~

~~three or more of said clock phases are selected by said phase selector and the data sampling is triggered by said three or more clock phases~~.

2. (Presently amended) A clock and data recovery circuit as claimed in claim 1, further comprising:

a counter coupled between said data sampling component and said phase selector, wherein said logic output statement of said data sampling component causes said counter to count up, count down or hold ~~wherein said reaction of said counter is counting up, counting down, or holding of the counter with the counter value transferred to the phase selector assigned to select the clock phases~~.

3. (Original) A clock and data recovery circuit as claimed in claim 1, wherein

the data signal is a binary signal having signal states zero or one defining a bit sequence.

4. (Original) A clock and data recovery circuit as claimed in claim 1, wherein

said buffer component comprises bistable multivibrators.

5. (Presently amended) A clock and data recovery circuit as claimed in claim 1, wherein

said buffer component comprises a first, a second and a third buffer portion each having a data input and a data output, with the data inputs of the three buffer portions coupled to ~~the~~ said first data input.

6. (Cancelled).

7. (Cancelled).

8. (Presently amended) A clock and data recovery circuit as claimed in claim ~~6~~ 1, further comprising a first output receiving the data signal from the buffer portion which is triggered by the clock phase ~~i~~ *i*,

wherein at least one of said data signal ~~and/or~~ and said timing signal is transmitted by said first output.

9. (Presently amended) A clock and data recovery circuit as claimed in ~~one of~~ claim 5, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector.

10. (Presently amended) A clock and data recovery circuit as claimed in claim 9, wherein

the phase detector further detects the signal state of the data signal at the clock phase ~~i~~ *i* of the previous cycle of the timing signal.

11. (Presently Amended) A clock and data recovery circuit as claimed in claim 1, further comprising

a low pass filter ~~assigned~~ coupled to said phase detector.

12. (Original) A clock and data recovery circuit as claimed in claim 1, further comprising

dual rail amplifiers.

13. (Presently amended) A method for clock and data recovery comprising <u>the steps of</u>:

- receiving a data signal of a first frequency;

- defining a timing signal of a second frequency;

- dividing a cycle of the timing signal into a number of ~~N signal~~ <u>N clock</u> phases;

- sampling a portion of said data signal by a data sampling component resulting in a binary number, said data sampling component comprising a buffer component buffering said data signal and comprising a phase detector;

- looking up said binary number in a truth table yielding a logic output statement; and

- transmitting said logic output statement to a ~~counter causing a reaction of said counter wherein the~~ phase selector ~~selects three of more of the clock phases and triggers the data sampling by said three or more clock phases~~<u>;</u>

<u>wherein the data signal is a binary signal having signal states zero or one defining a bit sequence and wherein said data signal is buffered by a first, a second and a third group of bistable multivibrators, triggered by a first clock phase i, a second clock phase j and a third clock phase k, respectively, resulting in a buffering of the state of said data signal at said clock phases i, j, and k.</u>

14. (Presently amended) A method as claimed in claim 13, wherein <u>said transmitting step comprises the steps of (a) incrementing, decrementing, or holding a counter value in response to</u> ~~as reaction on~~ said logic output statement of the truth table <u>and (b)</u> transferring the counter value to the phase selector ~~assigned to select the clock phases~~.

15. (Cancelled).

16. (Presently amended) A method ~~as claimed in claim 15,~~ for clock and data recovery comprising the steps of:

- receiving a data signal of a first frequency;
- defining a timing signal of a second frequency;
- dividing a cycle of the timing signal into a number of N clock phases;
- sampling a portion of said data signal by a data sampling component resulting in a binary number; said data sampling component comprising a buffer component buffering said data signal and comprising a phase detector;
- looking up said binary number in a truth table yielding a logic output statement; and
- transmitting said logic output statement to a phase selector;

wherein the data signal is a binary signal having signal states zero or one defining a bit sequence and wherein the buffer component is triggered by a first clock phase i, a second clock phase j and a third clock phase k, resulting in a buffering of the state of said data signal at said clock phases i, j, and k; and

wherein ~~further defining~~ the clock phases ~~j~~ j and ~~k~~ k are further defined by at least one of the equations:

~~- $j = i + N/2 - M$ and $k = i + N/2$ if i ≤ N/2 and~~

~~- $j = i - N/2 - M$ and $k = i - N/2 + M$ if i > N/2~~

$j = i + N/2 - M$ and $k = i + N/2$ if $i \leq N/2$ and

$\underline{j = i - N/2 - M}$ <ins>and</ins> $\underline{k = i - N/2 + M}$ <ins>if</ins> $\underline{i > N/2}$

with selecting a parameter M within 0 < ~~M~~ $\underline{M}$ < ~~N/2~~ $\underline{N/2}$.

17. (Presently amended) A method as claimed in claim ~~15~~ <ins>13</ins> or 16, further <ins>comprising the step of</ins>

transmitting <ins>at least one of</ins> said data signal ~~(74) and/or~~ <ins>and</ins> said timing signal by an output with the transmission triggered by the clock phase ~~i~~ $\underline{i}$.

18. (Presently amended) A method ~~as claimed in claim 15,~~ <ins>for clock and data recovery</ins> further <ins>comprising the steps of:</ins>

<ins>- receiving a data signal of a first frequency;</ins>

<ins>- defining a timing signal of a second frequency;</ins>

<ins>- dividing a cycle of the timing signal into a number of N clock phases;</ins>

<ins>- sampling a portion of said data signal by a data sampling component comprising a buffer component buffering said data signal and comprising a phase detector, said step of sampling further including</ins> detecting the state of the data signal at ~~the~~ <ins>a</ins> clock phase ~~i~~ $\underline{i}$ of the previous cycle of the timing signal<ins>,</ins> resulting in a four digit binary number having sixteen possible values<ins>;</ins> ~~and~~

<ins>- looking up said four digit binary number in a truth table yielding a logic output statement; and</ins>

<ins>- transmitting said logic output statement to a phase selector</ins>

~~looking up said binary number in said truth table at each cycle of the timing signal yielding said reaction of the counter~~.

19. (New) A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of *N* clock phases;

- a data sampling component sampling a portion of said data signal causing a logic output statement based on a truth table, said data sampling component comprising a buffer component for buffering said data signal and comprising a phase detector coupled to said buffer component,

wherein the phase detector further detects the signal state of the data signal at a clock phase *i* of the previous cycle of the timing signal; and

- a phase selector coupled to said data sampling component.

20. (New) A clock and data recovery circuit as claimed in claim 19, further comprising: a counter coupled between said <u>data sampling component</u> and said phase selector, wherein said logic output statement of said <u>data sampling component</u> causes said counter to count up, count down or hold.

21. (New) A clock and data recovery circuit as claimed in claim 19, wherein the data signal is a binary signal having signal states zero or one defining a bit sequence.

22. (New) A clock and data recovery circuit as claimed in claim 19, wherein

said buffer component comprises bistable multivibrators.

23. (New) A clock and data recovery circuit as claimed in claim 19, said buffer component comprising a first, a second and a third buffer portion each having a data input and a data output, with the data inputs of the three buffer portions coupled to said first data input.

24. (New) A clock and data recovery circuit as claimed in claim 19, further comprising a first output receiving the data signal from the buffer portion which is triggered by the clock phase *i*,

wherein at least one of said data signal and said timing signal is transmitted by said first output.

25. (New) A clock and data recovery circuit as claimed in claim 23, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector.

26. (New) A clock and data recovery circuit as claimed in claim 19, further comprising

a low pass filter coupled to said phase detector.

27. (New) A clock and data recovery circuit as claimed in claim 19, further comprising

dual rail amplifiers.

28. (New) A clock and data recovery circuit comprising:

- a first data input receiving a data signal of a first frequency;

- a clock defining a timing signal of a second frequency;

- a phase generator dividing a cycle of the timing signal into a number of *N* clock phases;

- a data sampling component causing a logic output statement based on a truth table, said data sampling component comprising a buffer component buffering said data signal and a phase detector; and

- a phase selector coupled to said data sampling component;

wherein said data signal is buffered by a first, a second and a third group of bistable multivibrators, triggered by a first clock phase *i*, a second clock phase *j*, and a third clock phase *k*, respectively, resulting in a buffering of the state of said data signal at said clock phases *i*, *j*, and *k*.